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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/029,198	12/28/2001	Jong Dae Kim	0465-0883P	5402

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EXAMINER	
NELSON, ALECIA DIANE	

ART UNIT	PAPER NUMBER
2675	

DATE MAILED: 03/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/029,198	KIM, JONG DAE	
	Examiner	Art Unit	
	Alecia D. Nelson	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-16,19 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1,3-16,19-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. ***Claims 1, 5, 11, 16, 19, and 20*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano et al. (U.S. Patent No. 6,529,181).

With reference to **claims 1, 11, and 16,** Nakano et al. teaches a liquid crystal display device comprising a LCD panel (10); a plurality of source drivers (130) applying data signals to the LCD panel; a plurality of gate drivers (140) applying gate driving signals to the LCD panel; a timing controller (100) outputting to the source drivers at least two clock signals (D4, 131; D5, 132) having different phases (see column 6, lines 30-37), the timing controller separately outputting RGB (134) data synchronized with

each output signal to the source drivers (see column 7, lines 15-23); and at least two data buses transmitting the data separately output from the timing controller to the source drivers (see column 6, line 30-column 7, line 23), wherein the at least two data buses are connected between the timing controller and the respective source drivers (see Figure 1), a number of data buses (131-133,141) are in proportion to a number of clock signals (D4, D5, D1, G1) output from the timing controller (100), and the source drivers (130) separately sample the data (see column 6, lines 21-63). With further reference to ***claims 11 and 16,*** Nakano et al. also teaches that the first clock signal (D4) is transmitted to odd-numbered drain drivers (130) and clock signal (D5) is transmitted to even numbered drain drivers (130) (see column 6, lines 38-43).

With reference to **claim 5,** Nakano et al. teaches that the fist and second clock signals (D4, D5) have opposite phase to each other (see column 6, lines 30-37).

With reference to **claims 19 and 20**, Nakano et al. teaches that the at least two data buses (131-133, 141) are separated from each other (see Figure 1).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. ***Claims 3, 4, 7-9, 12-15, 17, and 18*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano et al. (U.S. Patent No. 6,529,181) in view of Uchino (U.S. Patent No. 6,040,816)

With reference to **claims 3, 4, 12, and 14**, While Nakano et al. teaches all as required and explained above with reference to **claims 1 and 11**, there fails to be any teaching of the timing controller outputting data synchronized with the rising and falling edge time of each clock signal.

Uchino teaches that the data is synchronized with a rising edge time and falling edge time of each clock signal (see Figure 2).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the data to be synchronized with the rising and falling edge time of the clock signal as taught by Uchino in the system similar to that which is taught by Nakano et al. in order to thereby reduce noise and providing a clearer display to the user.

With reference to **claims 7, 8, 13, 15, 17, and 18,** While Nakano et al. teaches all as required and explained above with reference to **claims 1 and 11**, there fails to be any teaching of the source driver samples data in the falling edge time when the data synchronized with the rising edge timing or that the driver samples data in the rising edge time when the data synchronized in the falling edge timing is output.

Uchino teaches that the source driver samples data (A1-A3) synchronized with a rising edge of the data synchronized with a falling edge of each clock signal that is output (see Figure 2).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the data to be synchronized with the rising and falling edge time of the clock signal as taught by Uchino in the system similar to that which is taught by Nakano et al. in order to thereby reduce noise and providing a clearer display to the user.

With reference to **claim 9**, while Nakano et al. teaches a first clock signal (D4) for driving odd drain drivers and a second clock signal (D5) for driving even drain drivers (see column 6, lines 38-43), there fails to be any disclosure of the odd numbered display data output being synchronized with a rising edge of the first clock signal, or an even numbered display data synchronized with a rising edge of the second clock signal is output.

Uchino teaches that the source driver samples data (A1-A3) synchronized with a rising edge of the data synchronized with a falling edge of each clock signal that is output (see Figure 2).

Therefore it would have been obvious to one having ordinary skill in the art to allow for synchronization as taught by Uchino in a system which drives odd and even display data as taught by Nakano et al. in order to reduce the amount of crosstalk and thereby enhancing the resolution of the liquid crystal panel.

6. ***Claims 2, 6, and 10*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano et al. as applied to **claim 1** above, and further in view of Itakura (U.S. Patent No. 5,252,957).

With reference to **claim 2, 6, and 10** Nakano et al. teaches all that is required as explained above, however fail to specifically teach that the number of data busses is in proportion to the number of clock signals.

Itakura teaches an AMLCD wherein three busses carry three clock signals (CK1-3) and three different busses carry video data R, G, and B (see Figure 1). With further reference to claim 6, it is taught that the three clock signals have different phases to one another (see Figure 3).

Therefore it would have been obvious to one having ordinary skill in the art to allow the usage of the same amount of data busses as clock busses as taught by Itakura in a device similar to that which is disclosed by Nakano in order to thereby further reduce the amount of crosstalk n order to enhance the display qualities.

Response to Arguments

7. Applicant's arguments filed 11/09/05 have been fully considered but they are not persuasive. The applicant argues that Nakano and Uchino fails to disclose or suggest the timing controller separately outputting R/G/B data synchronized with each output signal to the source drivers and the source drivers separately sample the data to thereby reduce electricity consumption. However, it is the examiner's position that Nakano teaches the timing controller (100) separately outputting RGB data

synchronized with each output signal to the source drivers (see column 6, lines 21-29, column 7, lines 15-23). As to the newly recited limitation of the separate sampling of the data to reduce electricity consumption, the MPEP describes the limitation to be written in Functional Language, wherein if the structure is taught then it is an inherent function for the structure to obtain the same results (see MPEP 2114). Therefore, it is the examiner's position since Nakano teaches the structural limitations as recited in the claims the device would therefore reduce electricity consumption.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alecia D. Nelson whose telephone number is 571-272-7771. The examiner can normally be reached on Monday-Friday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 571-272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

adn/ADN
March 2, 2006

KENT CHANG
PRIMARY EXAMINER